REMARKS

In the Office Action, the Examiner rejected claims 1, 2, 4-8, and 10-29, which represent all pending claims in this application. With this Response, Applicant amends claims 1, 6, 10, and 16, and cancels claim 7. Applicant respectfully traverses the Examiner's rejections and submits that all claims, as amended, are allowable over the prior art.

Claim Rejections Under U.S.C. § 102

The Examiner rejected claims 1, 2, 4, 5, 10–21, and 26-29 under 35 U.S.C. 102(e) as allegedly anticipated by Hironaka et al., U.S. Application Publication No. 2004/0088489 ("*Hironaka*"). Applicant respectfully traverses these rejections.

With this Response, claim 1 has been amended to include the subject matter of claim 7, that is: "the TCache portion is indexed only when the processor executes one of: a branch instruction; a jump instruction; a call instruction; and a return instruction." In the Office Action mailed January 10, 2007, the Examiner rejected the subject matter of claim 7, citing *Hironaka* at Fig. 11, Ref. 31 as allegedly disclosing this feature. However, Applicant respectfully submits that *Hironaka* does not disclose "the TCache portion is indexed only when the processor executes one of: a branch instruction; a jump instruction; a call instruction; and a return instruction," either at Fig. 11, Ref. 31, or anywhere else in that application.

The cited reference in *Hironaka* refers to a branch predictor, which attempts to predict, before execution, the instruction path the processor will take. *See, e.g.*, *Hironaka*, ¶ [0142]. The branch predictor of *Hironaka* sends instruction addresses to

the Multi-port instruction/trace integrated cache **before** execution. *See Hironaka*, Fig. 11, "Predict path" step; Fig. 12, "Predict path" step. By contrast, the TCache as recited in claim 1 is indexed **only** when the processor executes a branch, jump, call, or return instruction. The TCache portion index is not updated before execution, as required by the multi-port instruction/trace integrated cache of *Hironaka*. Further, while *Hironaka* references branching generally (*see, e.g.*, *Hironaka*, ¶¶ [0174] and [0179]), *Hironaka* does not disclose indexing a trace cache upon execution of a branch instruction, or upon execution of a jump, call, or return instruction. In fact, *Hironaka* does not contain or suggest a single reference to jump, call, or return instructions. For at least these reasons, Applicant respectfully submits that *Hironaka* does not teach or suggest "the TCache portion is indexed only when the processor executes one of: a branch instruction; a jump instruction; a call instruction; and a return instruction," as recited in claim 1, as amended. Therefore, Applicant submits that claim 1 is allowable over the cited prior art for at least the above reasons.

Independent claims 10, and 16 have also been amended to include a limitation similar to that of claim 7 and therefore are allowable over the cited prior art for at least the same reasons as set forth above with respect to claim 1. Claims 2, 4, 5, 11-15, 17-21, and 26–29 each depend from one of allowable claims 1, 10, or 16, and therefore are also allowable for at least the same reasons.

Claim Rejections Under U.S.C. § 103

The Examiner rejected claims 6–8 and 22–25 under 35 U.S.C. § 103(a) as allegedly anticipated by *Hironaka* in view of Takashima et al., U.S. Patent No. 6,473,331 ("*Takashima*").1 Applicant respectfully traverses these rejections.

Claim 6 has been amended to include the subject matter formerly of claim 7. At page 9 of the Office Action, the Examiner relied solely on *Hironaka* as allegedly disclosing the limitation of former claim 7. However, as discussed in the preceding section, *Hironaka* does not, in fact, teach or suggest "the TCache portion is indexed only when the processor executes one of: a branch instruction; a jump instruction; a call instruction; and a return instruction," as recited in claim 6, as amended. *Takashima* does not cure this defect, nor has the Examiner asserted that it does. *Takashima* discloses a semiconductor memory device and various mounting systems, but does not disclose "the TCache portion is indexed only when the processor executes one of: a branch instruction; a jump instruction; a call instruction; and a return instruction," as recited in claim 6, as amended. In fact, *Takashima* does not disclose the concept of a trace cache at all.

Because neither *Hironaka* nor *Takashima*, nor the combination thereof, teaches or suggests all of the elements of claim 6, as amended, Applicant respectfully submits that claim 6 is allowable over the cited prior art for at least the above reasons.

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1 At page 8 of the Office Action, the Examiner lists Takashima as U.S. Patent No. 6,463,509. However, that patent number corresponds to a patent issued to Teoman et al. Applicant believes this to be a typographical error and wishes to make clear that all references to *Takashima* in this response refer to U.S. Patent No. 6,473,331.

Claims 8 and 22–25 depend from claim 6 and are therefore also allowable for at least the same reasons as claim 6.

Conclusion

In view of the foregoing amendments and remarks, Applicant submits that this claimed invention is neither anticipated nor rendered obvious in view of the cited prior art. Applicant therefore requests reconsideration of the application, and the timely allowance of the pending claims.

Please grant any extensions of time required to enter this response and charge any additional required fees to Deposit Account No. 06-0916.

Respectfully submitted,

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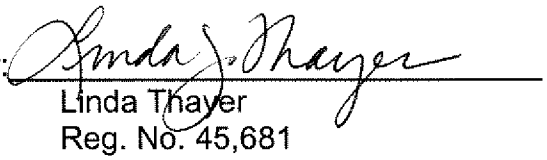
Dated: April 10, 2007

By: 
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